

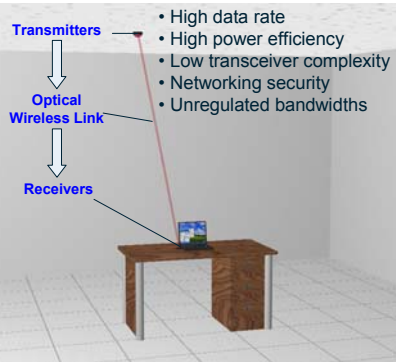


An Analog Front-End Receiver with Desensitization to Input Capacitance for Free Space Optical Communication

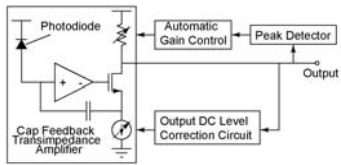


Yiling Zhang, Valencia Joyner
 Advanced Integrated Circuits and Systems Laboratory
 Tufts University, Department of Electrical and Computer Engineering

Optical Wireless Link

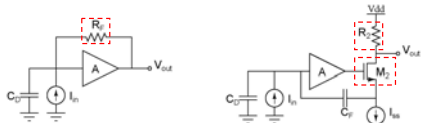


Front-End Amplifier Architecture



- Facilitate wide Field-of-View optical receiver with large Input parasitic capacitance.
- Achieve wide dynamic range to accommodate link distance and angle variation.

Resistive Feedback TIA vs. Capacitive Feedback TIA



Resistive feedback

Capacitive feedback

$$\text{Gain: } \frac{V_{out}}{I_{in}} = \frac{A}{A+1} R_F$$

$$\text{Gain: } \frac{V_{out}}{I_{in}} = \frac{(A+1) \cdot C_F}{C_D + (A+1) \cdot C_F} R_F$$

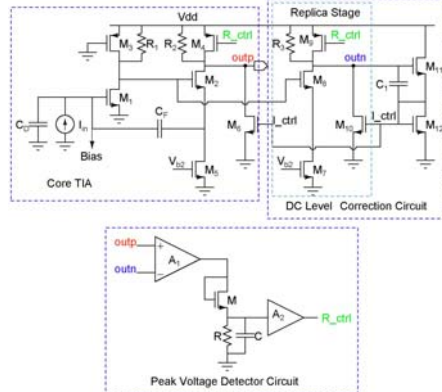
$$\text{BW: } f_{-3dB} = \frac{1}{2\pi R_F C_D} \frac{A+1}{g_{m2}}$$

$$\text{BW: } f_{-3dB} = \frac{1}{2\pi} \frac{(A+1)}{C_x} \frac{1}{g_{m2}}$$

$$C_x = \frac{1}{\frac{1}{C_D} + \frac{1}{(A+1) \cdot C_F}}$$

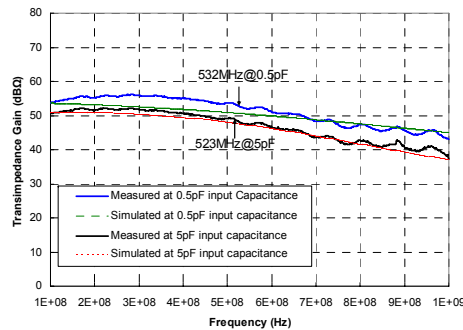
- No direct trade-off between Gain and BW for capacitive feedback topology.
- C_x is the series combination of C_D and $(A+1) \cdot C_F$, which gives $C_x < C_D$.

Capacitive Feedback TIA with Automatic Gain Control



- Capacitive feedback TIA splits the feedback node from the output node to eliminate the direct trade-off between gain and bandwidth.
- DC level correction circuit with a replica of output stage sets the output voltage level to a nearly constant value when the gain is varying.
- Peak voltage detector circuit with a differential pre-amplifier and a post amplifier is implemented to sense the output level and provide the AGC control signal.

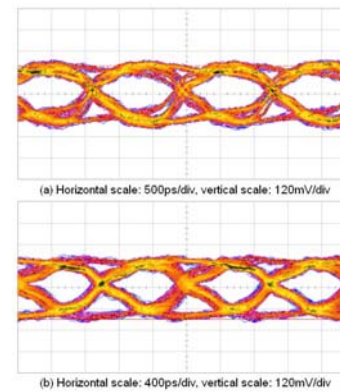
Measured and Simulated Frequency Response



$C_D = 0.5\text{pF}$ → $C_D = 5\text{pF}$
 BW=532MHz → BW=523MHz

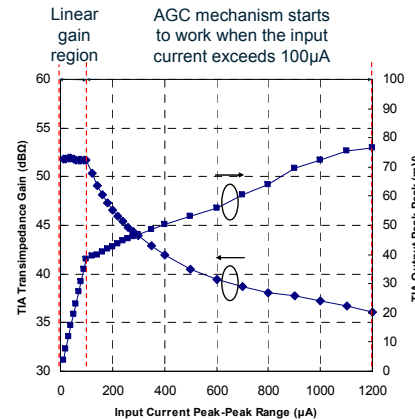
- Input capacitance increases by 10 times, bandwidth only decreases within 5%.
- The bandwidth is insensitive to the variation of input capacitance due to the capacitive feedback topology.

Electrical Test Eye Diagram

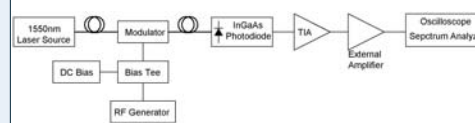


- (a) 50 μA peak-peak input current at 750Mbit/s.
- (b) 50 μA peak-peak input current at 1Gbit/s. Input current is patterned by a $2^{12}-1$ PRBS, Manchester-coded bit sequence.

Automatic Gain Control Performance

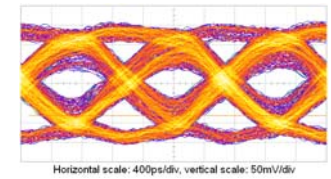


Optical Test Setup



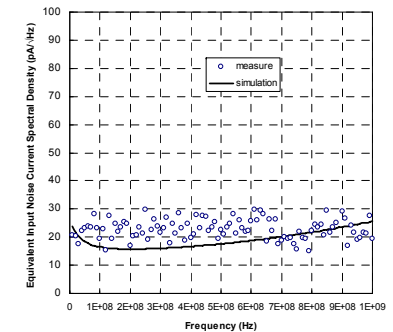
The incident light is modulated by RF signal with a $2^{12}-1$ PRBS, Manchester-coded data sequence.

Optical Test Eye Diagram



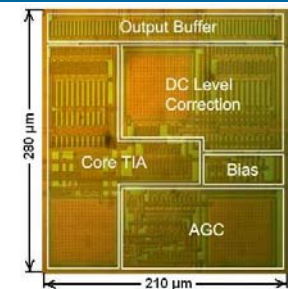
Measured eye diagram with 0dBm input optical power at 750Mbit/s.

Measured and Simulated Input Referred Noise



Input referred noise is 18.6pA/√Hz for 5pF input capacitance

Chip Microphotograph



Summary of Performance

Technology	AMI 0.5 μm CMOS
DC Gain	52dB Ω – 36dB Ω @ 5pF
-3-dB Bandwidth	523MHz @ 5pF 532MHz @ 0.5pF
Input Current Dynamic Range	42dB
Input Referred Noise	18.6pA/√Hz @ 5pF
Power Dissipation	53mW
Chip Area (without Pads)	210 μm \times 280 μm